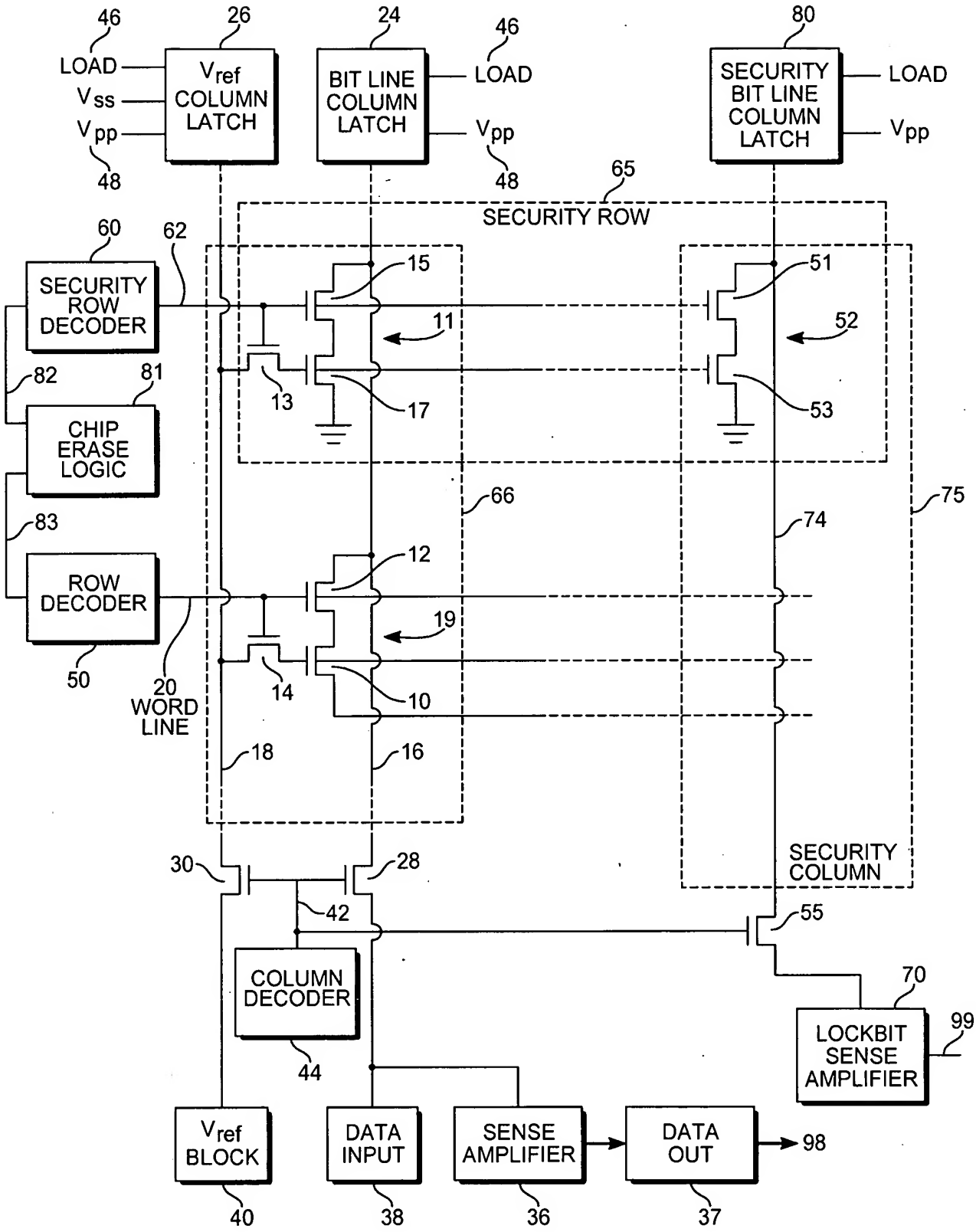
46
LOAD
Vss
Vpp
48
26
Vref COLUMN LATCH
24
BIT LINE COLUMN LATCH
46
LOAD
Vpp
48
80
SECURITY BIT LINE COLUMN LATCH
LOAD
Vpp
65
SECURITY ROW
60
SECURITY ROW DECODER
62
15
11
13
17
51
52
53
82
81
CHIP ERASE LOGIC
83
ROW DECODER
50
20
WORD LINE
66
12
19
14
10
18
16
75
74
SECURITY COLUMN
30
28
42
55
COLUMN DECODER
44
70
LOCKBIT SENSE AMPLIFIER
99
Vref BLOCK
40
DATA INPUT
38
SENSE AMPLIFIER
36
DATA OUT
37
98

Fig. 1